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This technical report has been reviewed and is approved for publication.

FOR THE COMMANDER

Raymond L. Loiselle

Raymond L. Loiselle, Lt.Col., USAF
Chief, ESD Lincoln Laboratory Project Office

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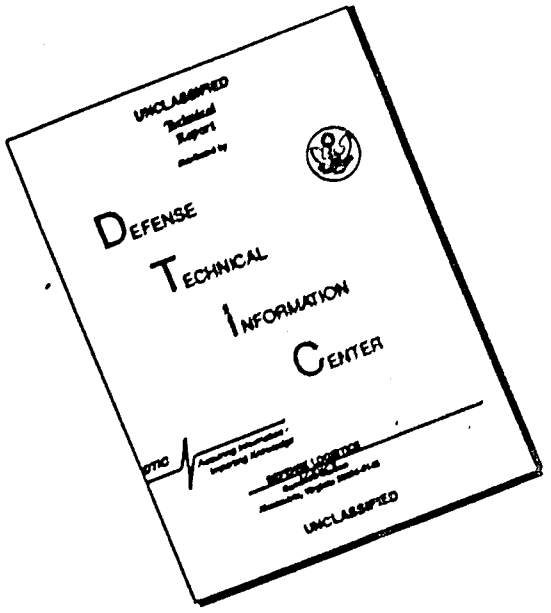

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INFORMATION PROCESSING TECHNIQUES PROGRAM

VOLUME I. PACKET SPEECH SYSTEMS TECHNOLOGY

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TO THE
DEFENSE ADVANCED RESEARCH PROJECTS AGENCY

1 APRIL — 30 SEPTEMBER 1980

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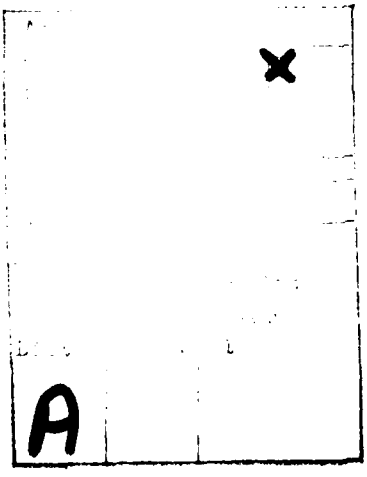
LEXINGTON MASSACHUSETTS

ABSTRACT

This report describes work performed on the Packet Speech Systems Technology Program sponsored by the Information Processing Techniques Office of the Defense Advanced Research Projects Agency during the period 1 April through 30 September 1980.



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INTRODUCTION AND SUMMARY

The long-range objectives of the Packet Speech Systems Technology Program are to develop and demonstrate techniques for efficient digital speech communication on networks suitable for both voice and data, and to investigate and develop techniques for integrated voice and data communication in packetized networks, including wideband common-user satellite links. Specific areas of concern are: the concentration of statistically fluctuating volumes of voice traffic; the adaptation of communication strategies to varying conditions of network links and traffic volume; and the interconnection of wideband satellite networks to terrestrial systems.

Previous efforts in this area have led to new vocoder structures for improved narrowband voice performance and multiple-rate transmission, and to demonstrations of conversational speech and conferencing on the ARPANET and the Atlantic Packet Satellite Network.

The current program has two major thrusts: i.e., the development and refinement of practical low-cost, robust, narrowband, and variable-rate speech algorithms and voice terminal structures; and the establishment of an experimental wideband satellite network to serve as a unique facility for the realistic investigation of voice/data networking strategies.

This report covers work in the following areas: filter bank vocoder development; design study of a high-speed, easily programmable, research-oriented speech processor; design and implementation of compact, modular packet voice terminals and local access area facilities; the design and implementation of a miniconcentrator facility to mediate the flow of local access area traffic onto a wideband channel; and experimental definition and planning for the wideband network.

An integrated noise-suppression module has been incorporated into a real-time software Belgard-vocoder implementation in a manner compatible with the LSI Belgard structure. The hardware design study for a high-speed F100K signal processor has been completed; the design meets the original goals of high throughput, ease of programming, and modest size. Second-generation versions of the Packet Voice Terminal (PVT) have been implemented and tested on the Lincoln experimental access network (LEXNET). Key new features include extended memory, DMA I/O, a flexible external vocoder interface port, and a microprocessor-controlled telephone-instrument subsystem. ST and NVP-2 protocol software have been developed for the PVTs. Miniconcentrator development has proceeded, including implementation of all software for critical gateway functions and development and test of a distant host hardware interface to the wideband satellite network. Satellite earth-station equipment for the wideband packet speech experiments has been installed and subjected to initial testing at Lincoln and at the other sites on the wideband network.

INFORMATION PROCESSING TECHNIQUES PROGRAM
VOLUME I: PACKET SPEECH SYSTEMS TECHNOLOGY

I. FILTER BANK VOCODERS

Negotiations were conducted with the Bell System to obtain some documentation on their Digital Signal Processing chips. The availability of such documentation would allow us to write programs to test the hypothesis that a total of two chips should be sufficient to implement the Belgard analyzer, and two more for the synthesizer. It would also be possible to assess the chip's capability for other vocoder-related functions, such as pitch extraction. Presently, it does not appear that the necessary information will be made available.

A real-time software version of the Belgard channel vocoder has been expanded to include an integrated acoustic-noise-suppression capability. Because the vocoder analyzer as realized in the Texas Instruments' custom LSI chip does not allow access to the bandpass filter outputs, some algorithm compromises are necessary if the Belgard hardware is to be potentially equipped with this feature. The modified noise-suppression algorithm is activated once per frame and is driven only by the quantized channel weights and the pitch information. Approximate signal-to-noise ratios (SNRs) are computed for all channels using this information, and the log channel weights are then attenuated appropriately via direct spectral subtraction. The noise-suppression module could be implemented in the control microprocessor firmware and inserted just prior to the parameter encoding routines. No multiplies are involved in the modified algorithm implementation.

Second-generation Belgard synthesizer devices were supplied by Texas Instruments for evaluation via the LDSP-based real-time test bed. Observed performance was, in general, markedly superior to that of earlier versions. Although some relatively minor anomalies were discovered which seem straightforward to solve, a major SNR problem remains. Subjective experiments with a calibrated attenuator suggested that an improvement on the order of 18 to 20 dB is warranted before the device could be considered usable. Processed speech recordings were forwarded to Texas Instruments for further study.

Some implementational studies have been initiated exploring the possibility of a compact, all-digital Belgard channel vocoder based primarily on the NEC μPD 7720 signal-processing-oriented single-chip microcomputer. Detailed preliminary documentation for this device has been obtained and has been studied in considerable detail. Delivery of EPROM versions of the device is currently projected for the first of the calendar year. These will apparently operate at a slightly reduced clock rate relative to the factory mask-programmed ROM versions. Initial indications are that a design comprised of five NEC chips in conjunction with a suitably chosen 8-bit single-chip μ-controller is feasible. Some attention is being focused on reducing the chip count of the analog conditioning and digital/analog interface subsystems. This may be possible through innovative application of commercial CODEC and CODEC filter devices. Work has also been initiated on a PDP-11/45-based cross-assembler for the 7720.

II. HIGH-PERFORMANCE PROGRAMMABLE SPEECH RESEARCH PROCESSOR

A study has been performed addressing the design of a high-speed signal processor as a potential successor to the LDSP. The basic design goals of the new machine include: throughput on the order of five times that of the LDSP, ease of programming, and modest size. Since the highest-performance commercially available digital technology base (ECL 100K) is only 2.5 times faster than the logic series used in the LDSP (ECL 10K), the desired increase in throughput must come from a combination of architecture and technology base.

The architecture developed supports a three-address, register-to-register ALU operation and a simultaneous two-read or one-write data memory access. The data memory communicates only with the general register file. Parallel index register manipulations are also performed simultaneously to reduce address generation overhead. A 24-bit word length was chosen as a compromise between increased computational precision and machine speed/complexity. The projected instruction cycle time is 40 ns, which will support all operations in a single epoch except integer multiplies and floating-point computations. The index, increment, I/O, and status registers will be accessible to the ALU as if they were general registers. Figure 1

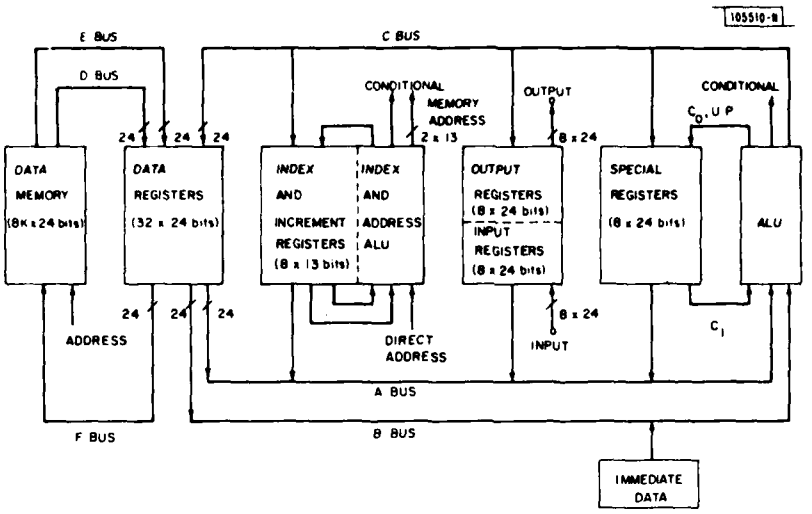

Fig. 1. Architecture of high-speed programmable speech research processor.

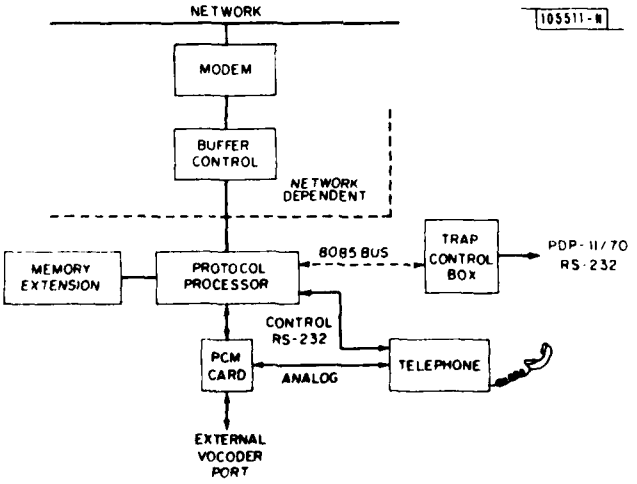

Fig. 2. System block diagram of Packet Voice Terminals with LEXNET and trap control card interfaces.

shows a block diagram of the machine architecture, including communication paths among the data memory, data registers, index and address complex, I/O registers, special registers, and ALU.

The structure will support an instruction of the form:

$$M \rightarrow R \quad ; \quad M \rightarrow R \quad ; \quad R \otimes R \rightarrow R$$

or

$$R \otimes R \rightarrow R \quad ; \quad R \rightarrow M$$

where M indicates an arbitrary data memory address, R a general register address, $\otimes$ an arbitrary ALU operation, and the direction of data transfer. ALU operations include the standard integer, logical, and floating-point repertoire with the exception of integer or floating-point divides. Several unique arithmetic instructions (e.g., multiply-accumulate) as well as a flexible set of control instructions are also included. Projections indicate that a hardware implementation will require six large, specially designed wirewrap panels and about 1000 F100K devices. Net complexity is on the order of 3 to 4 times that of the LDSP.

Detailed documentation of the design has been completed and will be distributed under separate cover as a Lincoln Technical Note (TN 1980-50).

III. PACKET VOICE TERMINAL AND LOCAL ACCESS AREA

A. Packet Voice Terminal

As previously reported, the Packet Voice Terminal (PVT) has been subjected to a major redesign addressing a variety of evolving requirements in the context of the Wideband Experimental Packet network and beyond. The new design is fundamentally a single CPU system featuring 8K bytes of local RAM, a flexible DMA type of in/out capability, an RS-232 serial ASCII I/O port to support miscellaneous control functions (e.g., telephone instrument), a 32K-byte program memory expansion option, an integrated 64-kbps PCM digital voice subsystem, and a powerful external vocoder interface port. The revised vocoder interface design takes advantage of efficient DMA transfers and has made the vocoder-handling microprocessor (referred to as μC-1 in past reports) unnecessary. An overall system block diagram of the PVT, together with its LEXNET and trap control box interfaces, is shown in Fig. 2. The revised protocol processor structure is shown in Fig. 3.

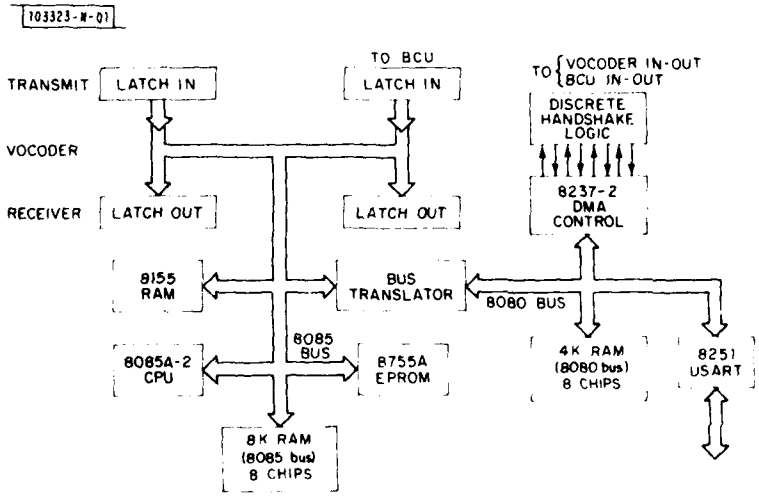

Fig. 3. Revised protocol processor structure.

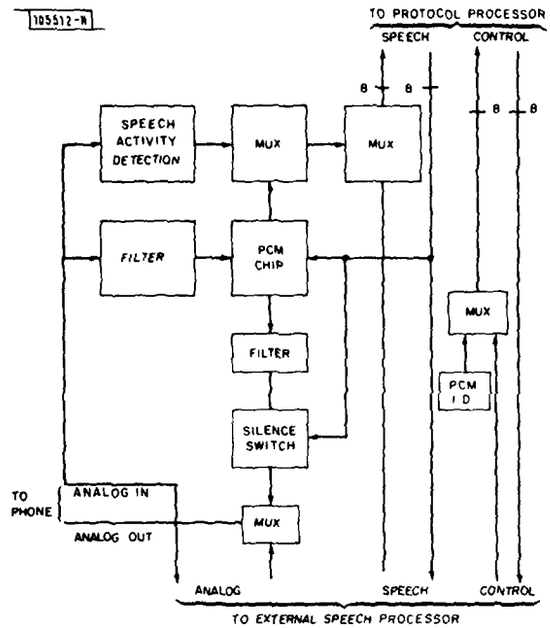

Fig. 4. PCM card and external speech processor interface.

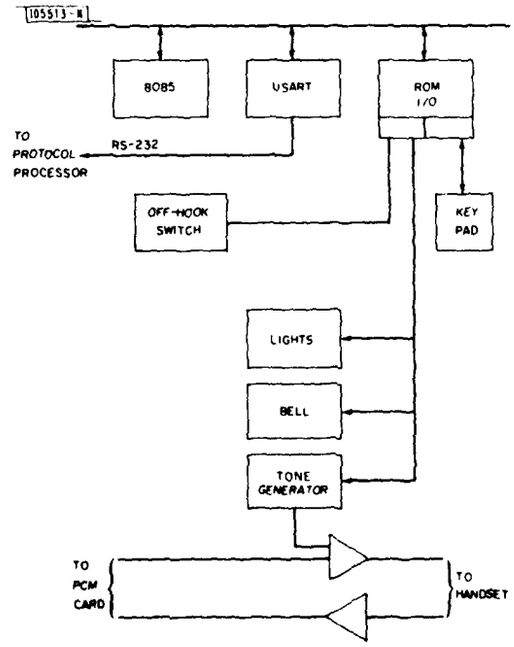

Fig. 5. Telephone-instrument subsystem block diagram.

The PCM voice subsystem, based on the INTEL 2910 CODEC chip family and mounted on a separate card, provides a backup digital voice mode through which the terminals can always communicate. The PCM card also serves as the physical location of the external vocoder interface and analog-signal distribution components. Analog connectivity to the telephone instrument is controlled by an on-card switch which routes the signals either to the PCM complex or to the external vocoder interface. The PCM complex also features a silence detection capability which can be enabled through an on-card switch. External vocoders will incorporate their own silence detection as appropriate. Figure 4 shows the PCM complex and its byte-parallel interface to the protocol processor.

Given the revised, DMA-oriented structure of the PVT I/O, a flexible external vocoder interface concept was developed to take advantage of the efficiencies offered by DMA transfers. Digital voice traffic to and from the external vocoder is handled in a byte-parallel fashion via a pair of 8-bit paths. Since the DMA is assumed to be continuously active, a full handshake is not necessary and word-transfer strobes are generated by the external device. The speech data are separated into packets through framing signals provided by the external vocoder. A simple packet format has been developed which incorporates silence detection and rate control information in the header field. A second pair of 8-bit paths is provided to support control functions such as the downloading of software into programmable speech processors.

A third card is used to house the 32K-byte program memory expansion option. The extra memory is provided to support more advanced and complex voice protocol software that may evolve in response to future needs.

A new design has been developed for the telephone-instrument subsystem itself. The telephone unit, physically external to and separate from the PVT subrack, contains a minimal configuration 8085 microprocessor complex which controls dialing and signaling functions. The digital control paths connect to the PVT CPU through the RS-232 serial link. The telephone μP interprets dialing keys and the off-hook condition. It also controls the dial tone, ringing tone, busy signal, and "bell." The special tones are generated by the controller hardware and added to the analog signal driving the earpiece. Analog-signal paths between the telephone and PCM card are of the balanced twisted-pair type. Figure 5 shows a block diagram of the telephone-instrument subsystem, and Fig. 6 shows the hardware as mounted in a standard-size telephone set.

Fig. 6. Telephone instrument and associated circuitry for PVT.

Four full PVT units, including their LEXNET interfaces, have presently been fabricated and tested. Two telephone instruments are operational, and two more await final checkout. Basic microcode has been generated allowing a pair of terminals to communicate on the LEXNET without NVP functions. This type of test verifies the basic functionality of all PVT subsystems. To exercise the external vocoder port, an LDSP-based real-time LPC-10 was developed and physically connected to the PVT. Appropriate timing signals were generated from the vocoder end through specialized LDSP software. In this way, point-to-point duplex 2400-bps speech communication was successfully demonstrated on the LEXNET, without higher-level voice protocols.

Work on the design of the software for the Packet Voice Terminals is reasonably mature. The protocols for point-to-point conversations have been written, keeping in mind future upgrades to include conferencing capabilities. ST and NVP-II protocols are being refined as actual implementation points up areas needing improvement.

In order to begin debugging before actual arrival of the revised PVTs, an experimental environment was devised using the EPOS operating system. Two copies of the PVT software are invoked. Protocol messages are sent between these two "terminals" via the ARPANET. The debugging configuration, which has also been invaluable in the development of miniconcentrator gateway code (see Sec. IV), is depicted in Fig. 7. Initial debugging of the NVP-II software in this environment is complete. This code, written in C, is now being linked to the assembly language code necessary to control the hardware subsystems of the protocol processor.

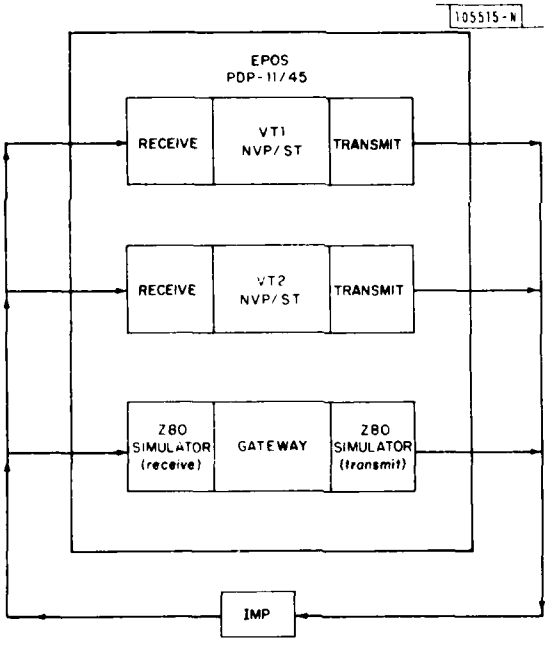

Fig. 7. Debugging configuration for PVT and miniconcentrator gateway software.

A capability for downloading 8085 software assembled on the PDP-11/70 to the PVT has been tested, and the major systems issues appear to have been resolved. An initial program consisting of a C portion and an assembly language segment written in "A Natural" were downloaded and linked to ROM-resident microcode code written in the INTEL asssembly language.

B. Access Area (LEXNET)

1. Modem

The modem card has been split into two pieces to allow the voice terminal to be located some distance from the main transmission cable. The cable tap contains the cable driver, receiver, and collision detection logic. It is contained in a 4⅝- × 2⅜- × 2-in. box which connects directly to a tee in the cable. The prototype of the cable tap contains two printed-circuit cards. Power is derived from a separate floating power supply in the terminal. The logic signals are optically isolated from the signals in the terminal to avoid ground-loop or lightning-surge problems typically resulting from long cable runs within a building. The prototype of the cable tap has been debugged and is working.

2. Buffer Control Processor

A new version of the program for the buffer control processor has been generated. Revisions include a 2-byte field for packet length specification as opposed to 1 byte. This program has been successfully tested with the concentrator interface port.

3. Trap Control Units

Three of the trap control units have now been built. They have been modified to allow downloading of software via a 9600-baud teletype link to the PDP-11/70. The link has been tested, and loading of code compiled on the PDP-11/70 has been demonstrated. The downloading path is being used for the development of the NVP software for the PVT.

4. Concentrator Interface Port

The concentrator interface port from the LEXNET has been interfaced to the SIO port of the UMC-Z80. Packets have been successfully sent back and forth over the RS-422 link between the LEXNET and UMC-Z80 at a 750-kbps rate. Unexpected hardware difficulties involving the interaction between the SIO chip and the DMAs in the Z80 have so far prevented us from achieving higher rate full-duplex communication on this RS-422 link.

5. Local Access Network Software

A new packet format for the LEXNET has been designed. It will allow for conference addressing capable of supporting up to eight conferences on a net. It also provides for control packets to allow communication among the various processors within a terminal. These packets will be used to control the conference addressing and to pass flow control information. The new format, which will require only minor software modifications, will be incorporated in the next version of the terminal software.

IV. MINICONCENTRATOR DEVELOPMENT

Progress continues on the implementation and checkout of all components of the miniconcentrator. Operational status of a full LEXNET-to-ARPANET gateway is imminent, and the requisite hardware and software interfaces for a LEXNET-to-WB SATNET gateway are operational and ready for further testing when the satellite channel becomes available (expected in early FY 81). The previous semiannual described in some detail the hardware and software design for the miniconcentrator system, as well as the internet voice protocols (ST and NVP-2) to be implemented. These designs remain essentially as described there. Status updates on the ongoing development of hardware interfaces and miniconcentrator gateway software are given in the following sections.

A. *Interface Hardware and Software Status*

The design and development of the special I/O board to interface the UMC-Z80 to the PSAT using the ARPANET Distant Host (DH) protocol have been completed. The interface circuitry includes handshaking logic, serial/parallel and parallel/serial conversion, tri-state data busing, byte-swap reformatting, and error detection logic. A functional block diagram of the

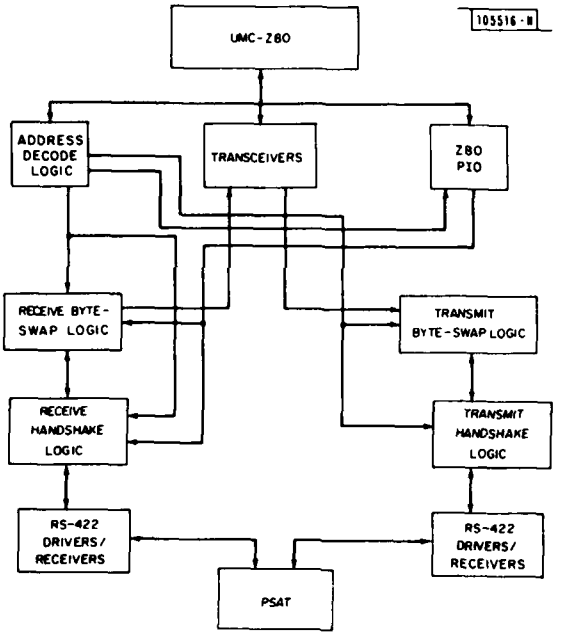

Fig. 8. Functional block diagram of DH interface card.

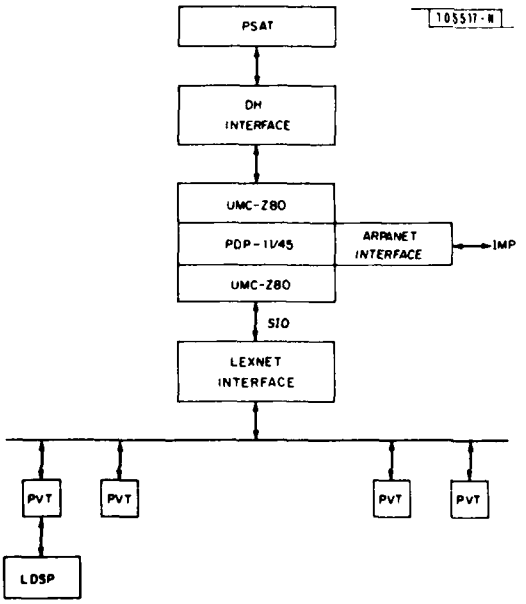

Fig. 9. Speech access facility configuration.

DH interface board is shown in Fig. 8. The circuits are mounted on a special PDP-11 compatible wirewrap board, and special RS-422 elements are included to allow communication via balanced twisted-pair cabling. The interface board includes about 60 integrated-circuit chips. Two units have been constructed and debugged, and one of these has been delivered to ISI. Construction of additional copies of the board for the other wideband network sites is under way. In order to check out the boards, a series of Z80 diagnostic programs was written to exercise all the functions of the board and to perform loopback tests with and without the PSAT. Loopback testing with the PSAT has been successfully carried out using Z80 programs written to exchange setup messages, status messages, and datagrams with the PSAT using the Host Access Protocol (HAP) designed by BBN. This HAP protocol will be used for packet communication between the miniconcentrator gateway and the PSAT for forthcoming experiments on the wideband channel.

Communication between the UMC-Z80 and the LEXNET is accomplished using the UMC-Z80's serial I/O (SIO) chip and a special LEXNET interface. A series of UMC-Z80 programs has been written to check out and debug this interface. Most of these programs have been run under the UNIX operating system using the manufacturer-supplied UMC-Z80 debugger (ZDB). The actual miniconcentrator code will run in the EPOS operating system environment. To make this possible, ZDB has been successfully modified to run under EPOS. The basic Z80 code for the miniconcentrator has been written, and has been tested in the EPOS environment.

Communication between the Z80 and the PDP-11 requires no special interface, since the PDP-11 can directly address Z80 memory. The required software to effect this communication has been written and tested using ZDB. Essentially the same software will be used for PDP-11 interchanges, with the two Z80's on the LEXNET and PSAT sides of the gateway.

B. Miniconcentrator Software Status

The development and checkout of the EPOS support environment for the miniconcentrator have been completed. EPOS can now be installed on the PDP-11/45 either directly from disk or downloaded from the PDP-11/70. An ARPANET communication package has been developed to allow communication among PDP-11 EPOS processes on the ARPANET. This software is an operational part of the LEXNET-to-ARPANET gateway, and has served in the interim as an essential development and debugging aid for the gateway and PVT software. Miniconcentrator software checkout has proceeded using the PDP-11/45's at both Lincoln and ISI. Access to the ISI computer over the ARPANET from Lincoln has been particularly helpful during morning hours (East Coast time).

Software for the PDP-11 and UMC-Z80's to execute all basic gateway functions has been written. Critical PDP-11 functions include the sorter, the ST forwarder/aggregator, the IP forwarder, the dispatcher, and the connection manager. The resource allocator and ST and IP routers are not critical to an initial communications capability on the WB SATNET, but these components have been designed, and coded in skeletal form. The status of the Z80 interface code for the miniconcentrator was described above. Using the ARPANET and EPOS debugging environment, two instances of PVT programs running in the PDP-11/45 at ISI have established ST connections via an IP/ST gateway running in the PDP-11/45 at Lincoln.

The initial checkout and demonstration of the full gateway capability will be comprised of a voice call setup and LPC conversation between a PVT on the LEXNET and a PDP-11 host and AP-120B speech processor combination at ISI. The speech access facility configuration shown in Fig. 9 is being used. The ARPANET interface allows communication with ISI for gateway and protocol checkout prior to the availability of the wideband channel, which will be accessed through the DH interface as shown. LPC is implemented in an LDSP at Lincoln and an AP-120B at ISI. Operational status of the full LEXNET-to-ARPANET gateway capability required to achieve this milestone is imminent. The same gateway software, together with the PSAT interfaces described above, will be used for initial packet speech experiments on the WB SATNET.

V. EXPERIMENT DEFINITION AND PLANNING

A current Supplement to the Experiment Plan is in preparation. As in the past, the Supplement will include a brief summary of the purposes and background of the Experimental Wideband Network Program. It will go on to provide up-to-date

information on the status of the three major aspects of planning and preparation for the program — namely, experimental system development and installation, system validation, and advanced systems experiments. Each of the major experimental network subsystems will be discussed under the first two topic areas, including the earth station and channel; ESI; PSAT; the PDP-11 concentrator and its special interfaces; the Voice Funnel; and the LEXNET and related packet speech access facilities. The third topic area will describe the progress of the past year in planning advanced systems experiments in broadcast satellite demand assignment, multi-user packet speech techniques, rate-adaptive communications, and digital voice conferencing. The Supplement will also include current schedule information for system development and validation and for the experimental programs. A few key items relevant to progress on system installation and integration are summarized briefly below.

The Western Union earth stations have been installed at all four sites. The installations at DCEC and SRI have been completed, and those stations are essentially ready for acceptance testing; checkout and alignment of the electronics are

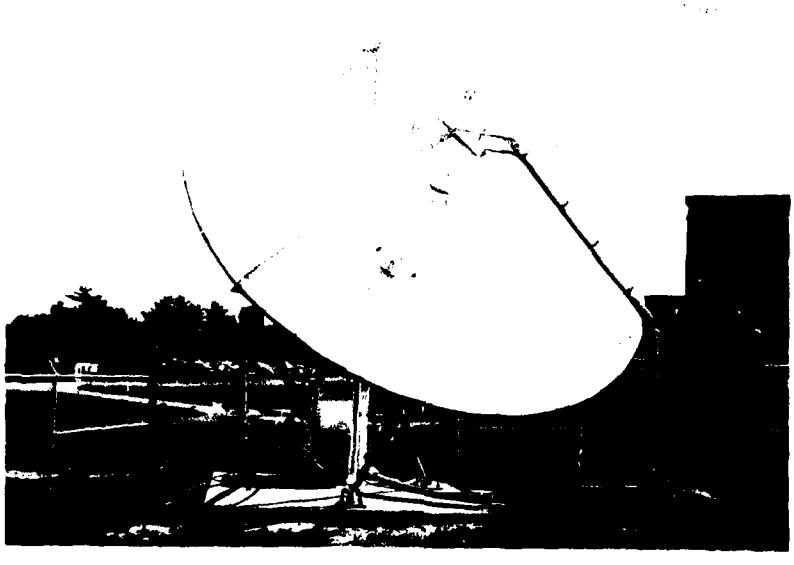

Fig. 10. Lincoln Laboratory earth terminal (outdoor portion).

nearing completion at ISI and Lincoln. The satellite network uses a portion of a transponder leased from Western Union on WESTAR III, which is in geostationary orbit at 91° West longitude. A photograph of the outdoor portion of the Lincoln earth station is shown in Fig. 10. The 5-m antenna and the earth station equipment were manufactured for Western Union by Scientific-Atlanta. The low-noise receiving amplifier, located in the antenna feed, operates at a downlink frequency of 3.731 GHz. The HPA is a 75-W traveling-wave-tube amplifier, operating at an uplink frequency of 5.959 GHz; it is located in the white air-conditioned fiberglass enclosure visible below the dish, with its modulator and the 84-MHz driver and receiver electronics for the 1500-ft IF cable runs connecting the earth station with the burst modem in the Group 24 laboratory area. Electric de-icing is provided for the dish and the Cassegrainian subreflector, both to insure reliable service in winter and to avoid the adjacent-satellite interference that could be caused by antenna pattern degradation due to ice deposits.

While it may seem that the installation of such a station should be a simple matter of plugging in and turning on a standard set of off-the-shelf commercial equipment, there is in fact a substantial amount of variation from site to site which requires special engineering attention to matters such as lengths and parameters of waveguide and coaxial cable runs, local RF environment, and so on.

The Lincoln PSAT has been delivered and installed. Basic PSAT software has been successfully run by BBN using control communications over the ARPANET. Packets have been exchanged between a UMC-Z80 and the PSAT using Lincoln's special DH interface board. ISI's PSAT was first delivered to Linkabit, where checkout of the PSAT/ESI interface was carried out; that PSAT is now installed at ISI. The installation of ESIs at ISI and Lincoln is imminent, after which integration and checkout of the WB SATNET will proceed.

A Wideband System Integration Meeting was held on 19 June 1980 at DCEC, in Reston. The meeting was organized by Lincoln Laboratory and was attended by representatives of the four experiment sites, the subsystem suppliers, the sponsoring agencies, and the satellite system integration contractor (COMSAT). The main purpose of the meeting was to address the specific near-term problems of assembling and debugging the equipment configurations at the sites. The four subsystem suppliers (Western Union, Linkabit, BBN, and — with respect to the miniconcentrator — Lincoln Laboratory) had prepared and circulated summaries of equipment physical and electrical requirements in advance. Topics discussed at the meeting included: delivery and installation schedules; subsystem interface definition issues; racks and cables; acceptance and integration test planning; and implications for near-term experiments. A summary of action items and unresolved issues was prepared by COMSAT and was distributed to the meeting attendees. Interaction on these items has continued as appropriate. The need for another integration meeting will be accommodated by suitable agenda items at the Wideband Meeting scheduled for 6 and 7 November 1980 at ISI.

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network speech	ARPANET	homomorphic vocoding

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

This report describes work performed on the Packet Speech Systems Technology Program sponsored by the Information Processing Techniques Office of the Defense Advanced Research Projects Agency during the period 1 April through 30 September 1980.

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